FORM PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
AVI99-01	09/316,699
APPLICANT: William J. Dally et al.	
FILING DATE: 05-21-99	GROUP: ~~2781~~ 2662

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
AV	AA	4,933,933	06-12-90	Dally et al.	~~370~~	~~60~~	
AV	AB	5,088,091	02-11-92	Schroeder et al.	~~370~~	~~94.3~~	
AV	AC	5,134,690	07-28-92	Samatham	395	200	
AV	AD	5,172,371	12-15-92	Eng et al.	~~370~~	~~60~~	
AV	AE	5,408,469	07-18-95	Opher et al.	~~370~~	~~60.1~~	
AV	AF	5,444,701	08-22-95	Cypher et al.	~~370~~	~~60~~	
AV	AG	5,521,591	05-28-96	Arora et al.	340	826	
AV	AH	5,532,856	07-02-96	Li et al.	359	118	
AV	AI	5,581,705	12-03-96	Passint et al.	395	200.13	
AV	AJ	5,583,990	12-10-96	Birrittella et al.	395	200.01	
AV	AK	5,617,577	04-01-97	Barker et al.	395	800	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO
	AL							
	AM							
	AN							
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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

AV	AR	Glass, Christopher J. et al., "The Turn Model for Adaptive Routing," Proceedings of the 19th International Symposium on Computer Architecture, May 1992, pp. 278-287.
AV	AS	R. Rettberg et al., "Development of a Voice Funnel System: Design Report," Report No. 4098, August 1979, 149 pages.
AV	AT	Dally, William, "Network and Processor Architecture for Message-Driven Computers," Chapter 3, VLSI and Parallel Computation, Edited by Robert Suaya et al., 1990, pp. 140-222.

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AV	AA2	5,659,716	08-19-97	Selvidge et al.	395	500	
AV	AB2	5,659,796	08-19-97	Thorson et al.	395	200.71	
AV	AC2	5,355,372	10-11-94	Sengupta et al.	~~370~~	~~60.1~~	
	AD						
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	AJ						
	AK						

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AV	AU	Dally, William, "Virtual-Channel Flow Control," IEEE Transactions on Parallel and Distributed Systems, March 1992, pp. 194-205.
AV	AV	Dally, William et al., "The Torus Routing Chip," Distributed Computing, (1996) 1: pp. 187-196.
AV	AW	Jesshope, Chris, "The MP1 Chip and its Application" Department of Electronic and Electrical Engineering, University of Surrey, Guildford, Surrey, GU2 5XH, UK pp. 47-54.

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aV	AX	Kessler, R.E., et al., "CRAY T3D: A New Dimension for Cray Research," IEEE, 1993, pp. 176-182.
aV	AY	Dally, William, et al., "Deadlock-Free Message Routing in Multiprocessor Interconnection Networks," IEEE Transactions on Computers, Vol. C-36, No. 5, May 1987 pp. 547-553.
aV	AZ	Jesshope, Chris, et al., "The MP1 Network Chip," IEEE, 1992 pp. 338-348.
aV	AR2	Dally, William J. et al., "The Reliable Router: A Reliable and High-Performance Communication Substrate for Parallel Computers," Proceedings of Parallel Computer Routing and Communication Workshop, Seattle, WA, May, 1994 , pp 241-255.
aV	AS2	Dally, William J. et al., "Architecture and Implementation of the Reliable Router," Proceedings of Hot Interconnects II, Stanford, CA, August 11-13, 1994, pp 122-133.
aV	AT2	Nuth Peter et al., "The J-Machine Network" Proceedings of the International Conference on Computer Design: VLSI in Computers and Processors, Cambridge, MA, October 1992, pp. 420-423.
aV	AU2	Dennison, Larry R., "The Reliable Router: An Architecture for Fault Tolerant Interconnect", Ph.D. Thesis, MIT, Cambridge, MA, June 1996, pp. 1-444.

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AV	AV2	Parulkar, G., et al., "a^{I}t^{P}m: A Strategy for Integrating IP with ATM," Computer Communications Review, Vol. 25, No. 4, 10-1-95, pp. 49-58.
AV	AW2	Robertazzi, T., et al., "Deflection Strategies for the Manhattan Street Network," Communications - Rising to the Heights, Denver, June 23-26, 1991, Vol. 3, 10-23-91, pp. 1652-1658, IEEE.
AV	AX2	Yang, C.S., et al., "Fault Tolerant Wormhole Routing In Hypercube Multicomputers," Microprocessing and Microprogramming, Vol. 35, No. 1/5, 09-01-92, pp. 667-672.
AV	AY2	Stunkel, C.B., et al., "The SP2 High-Performance Switch," IBM Systems Journal, Vol. 34, No. 2, 1995, pp. 184-204.
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